**Summary of Lesson Plan**

Name of College: GOVT. PG NEHRU COLLEGE, JHAJJAR

ACADEMIC SESSION: 2025-2026 For the Month of July 2025– December 2025

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| S.N. | Name of Assistant/ Associate Professor | SUBJECT/CLASS/ SEMESTER | TOPIC/ Chapters to be covered |
| 1 | PARDEEP | **B.C.A.**  **1st Semester**Computer Architecture | **July:** Digital Principles: Definition for Digital signals, Digital logic, Digital computers, Von Neumann Architecture, Boolean Laws and Theorems, K-Map: Truth Tables to K-Map, 2, 3 and 4 variable K Map, K-Map Simplifications, Don’t Care Conditions, SOP and POS.**August:** Number Systems: Decimal, Binary, Octal, Hexadecimal, Number System Conversions, BinaryArithmetic, Addition and subtraction of BCD, Octal Arithmetic, Hexadecimal Arithmetic, Binary Codes, Decimal Codes, Error detecting and correcting codes, ASCII, EBCDIC, Excess3Code, The Gray Code.**Assignment 1 and Class Test****September:** Combinational Circuits: Half Adder and Full Adder, Subtractor, Decoders, Encoder, Multiplexer, Demultiplexer Sequential Circuits: Flip-Flops- SR Flip- Flop, D Flip-Flop, J-K Flip-Flop, T Flip-Flop. Register: 4 bit register with parallel load, Shift Registers- Bidirectional shift register with parallel load Binary Counters-4 bit synchronous and Asynchronous binary counter.**Assignment 2****October:** Basic Computer Organization and Design: Instruction Codes, Computer Registers, ComputerInstructions, Timing and Control, Instruction Cycle, Memory-Reference Instructions, Input Output Interrupt, Complete Computer Description, Design of Basic Computer, Design of Accumulator logic. Central Processing Unit: Introduction, General Register Organization, Stack Organization, Instruction Formats, Addressing Modes, Data Transfer and Manipulation,Program Control, Reduced Instruction Set Computer (RISC), RISC Vs CISC. **Class Test****November:** Pipeline and Vector Processing: Parallel Processing, Pipelining, Arithmetic Pipeline, InstructionPipeline, RISC Pipeline. Input-Output Organization: Peripheral Devices, Input-Output Interface, Asynchronous data transfer, Modes of Transfer, Priority Interrupt, Direct memory Access, Input-Output Processor (IOP). Memory Organization: Memory Hierarchy, Main Memory, Auxiliary memory, AssociateMemory, Cache Memory, Virtual Memory, Memory Management Hardware.**Class Test and Discussion** |

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| 1 | PARDEEP | **M.Sc. C.S.** **1st Semester**Computer Organization and Architecture | **July:** Representation of Information: Number Systems: Binary, Octal and Hexadecimal, Integer and Floating-point representation, Character codes: ASCII and EBCDIC.**August:** Basic Building Blocks and Circuit Design: Boolean Algebra and Logic Gates: OR, AND, NOT, XOR Gates; De Morgan’s theorem; Universal building blocks; Simplifying logic circuits: sum of product and product of sum form; Karnaugh Map simplification; Combinational logic blocks (Adders, Multiplexers, Encoders, Decoder), Sequential logic blocks (Latches, Flip-Flops, Registers, Counters).**Assignment 1 and Class Test****September:** Register transfer and Micro-operations: Register Transfer Language; Bus and memory Transfer; Micro operations: Arithmetic, Logic & Shift Micro operations. Basic Computer Organization and Design: Instructions Codes, Register reference, Memory Reference & Input-Output instructions, Instruction Cycle, Timing and Control, Interrupts; Design of Control unit: Hardwired control unit, Micro-programmed control unit. Register Organization: General Register Organization, Stack Organization, Instruction Formats, Addressing Nodes; Data Transfer & Manipulation Instructions. Introduction to x86 Assembly Language programming.**Assignment 2****October:** Memory Organization: Memory Hierarchy, Main Memory, Auxiliary Memory, Cache Memory, Virtual Memory. Input-Output Organization: Peripheral Devices, Input-Output interface, Asynchronous Data Transfer, Modes of transfer, Priority interrupt, Direct Memory Access (DMA), input-output processors (IOP), Serial communication.**Class Test****November:** Parallel Computing: CISC and RISC - Features and Comparison, Pipeline and Vector Processing: Parallelprocessing, Pipelining, Arithmetic Pipeline, Instruction pipeline and Arrays Processors. Advanced Architecture Multi-processors, characteristics of multi-processors, Interconnection structures, Inter- processor Arbitration, Inter-processor Communication and Synchronization, Cache Coherence.**Class Test and Discussion** |

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| 1 | PARDEEP | **M.Sc. C.S.** **3rd Semester**Computer Security | **July:** Fundamentals of Computer Security: Overview of Computer Security: Key Concepts and Importance,Security Threats and Vulnerabilities: Malware, Phishing, Ransomware, Access Control Models: Discretionary,Mandatory, and Role-Based Access Control (RBAC), Cryptographic Principles: Symmetric and AsymmetricEncryption, Digital Signatures, Case Studies: Notable Cyber Attacks and their Impact.**August:** Secure Systems and Applications: Secure Software Development Practices, Operating System Security: Process Isolation, Secure Boot, Anti-malware Tools, Database Security: SQL Injection Prevention, Role-based Access, Application Security: OWASP Top 10 and Secure APIs, Penetration Testing and Vulnerability Assessment.**Assignment 1 and Class Test****September:** Network and Wireless Security: Network Security Fundamentals: Firewalls, IDS/IPS, VPNs, Wireless Network Security: WEP, WPA/WPA2, Emerging Protocols.**Assignment 2****October:** Secure Network Design: Zero Trust Architecture, Threat Monitoring and Incident Response, Case Studies: Securing IoT Devices. Advanced Topics and Legal Aspects: Emerging Threats: Quantum Computing in Cryptography.**Class Test****November:** AI in Cybersecurity, Blockchain for Secure Transactions, Digital Forensics and Cybercrime Investigation, Cybersecurity Laws and Frameworks: GDPR, HIPAA, NIST, Security Management: ISO 27001 Standards.**Class Test and Discussion** |